Claims:

1. A semiconductor memory including a semiconductor substrate where an active circuit element is formed, a plug formed in an interlayer insulator film formed on the semiconductor substrate and reaching to a surface of the interlayer insulator film, and a capacitor having a barrier layer, a lower electrode, a capacitor dielectric film of a ferroelectric material or a high dielectric material, and an upper electrode, which are stacked in the named order on the plug, wherein said barrier layer has a multilayer structure having at least three layers, which include a layer of a first metal in contact with a surface of said plug or said surface of said interlayer insulator film, a layer of a second metal in contact with said lower electrode, and at least one film of a metal nitride between said layer of said first metal and said layer of said second metal.

2. A semiconductor memory claimed in Claim 1, wherein said film of said metal nitride is formed of a nitride of said first metal or said second metal.

3. A semiconductor memory claimed in Claim 1, wherein said lower electrode is formed of at least one selected from the group consisting of platinum metal elements including Ru and Ir and conductive oxides of platinum metal elements.

4. A semiconductor memory claimed in Claim 1, wherein said first metal and said second metal are formed by one combination selected from the group consisting of :

Ti and Ti

Ti and Ta

Ta and Ti, and

Ta and Ta.

5. A semiconductor memory claimed in Claim 1, wherein said second metal is Pt and said second metal is Ti or Ta.

6. A semiconductor memory claimed in Claim 5, wherein said metal nitride film is TiN or TaN.

7. A semiconductor memory claimed in Claim 1, wherein said plug is formed of mainly W.

8. A semiconductor memory claimed in Claim 1, wherein said capacitor dielectric film is one formed by a sputtering or a solgel method.

9. A semiconductor memory claimed in Claim 1, wherein said capacitor dielectric film is one formed by a chemical vapor deposition process.

10. A semiconductor memory claimed in Claim 9, wherein said capacitor dielectric film is one deposited at a film deposition temperature of not greater than 500 degrees Celsius.

11. A semiconductor memory claimed in Claim 9, wherein said capacitor dielectric film is one deposited at a film deposition temperature of not greater than 475 degrees Celsius.

12. A semiconductor memory including a capacitor formed above a semiconductor substrate, the capacitor including a capacitor dielectric film located between a lower electrode and an upper electrode, the lower electrode being formed on a barrier layer in contact with the barrier layer and being electrically connected through a conductive member to an underlying layer, wherein said barrier layer has at least three layers, which include a layer of a first metal, one film of a metal nitride and a layer of a second metal, which are formed in the named layer counted from a lower position.

13. A semiconductor memory claimed in Claim 12, wherein said film of said metal nitride is formed of a nitride of said first metal or said second metal.

14. A semiconductor memory claimed in Claim 12, wherein a conductive cap layer is formed on said upper electrode, and said upper electrode is contacted with an upper level interconnection or connected through a via hole to said upper level interconnection.

15. In a process for fabricating a semiconductor memory, a process of forming a capacitor on a semiconductor substrate, comprising the steps of:

forming a barrier layer having a lower surface connected to an upper end of a conducting member having a lower end connected to an underlying layer;

forming a lower electrode on said barrier layer;

forming a dielectric film on said lower electrode; and

forming an upper electrode on said dielectric film,

wherein said step of forming said barrier layer includes the step of forming a first metal film, a metal nitride film and a second metal film in the named order.

16. A process for fabricating a semiconductor memory, claimed in Claim 15,

wherein said conducting member is formed in an interlayer insulator film formed on said semiconductor substrate, said upper end of said conducting member reaching a surface of said interlayer insulator film, and said lower end of said conducting member reaching a underlying conducting layer or a surface of said semiconductor substrate,

wherein said capacitor is formed by depositing said barrier layer, said lower electrode, said dielectric layer and said upper electrode on said surface of said interlayer insulator film in the named order to form a laminated film, and by patterning the laminated film so as to form said capacitor having said lower electrode electrically connected through said barrier layer to said conducting member, and

wherein said step of forming said barrier layer includes the steps of:

forming said first metal film on said surface of said interlayer insulator film to form a lowermost layer of said barrier layer;

forming said metal nitride film on said first metal film; and

forming said second metal film on said metal nitride film to form an uppermost layer of said barrier layer.

17. A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said metal nitride film is formed of a nitride of a metal element constituting said first metal film or said second metal film.

18. A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said first metal film, said metal nitride film and said second metal film are formed by one combination selected from the group consisting of :

Ti, TiN and Ti

Ti, TaN and Ta

Ta, TaN and Ti,

Pt, TiN and Ti,

Pt, TaN and Ta, and

Pt, TaN and Ti.

19. A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said lower electrode is formed of at least one selected from the group consisting of Ru, Ir, Ru oxide, Ir oxide and $SrRuO_3$.

20. A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said step of forming said barrier layer includes the steps of:

forming said first metal film on said surface of said interlayer insulator film;

forming said metal nitride film on said first metal film;

forming on said metal nitride film a predetermined number of multilayer film(s) each formed of a metal film and a metal nitride film; and

forming said second metal film on said predetermined number of multilayer film(s) to form said uppermost layer of said barrier layer.

21. A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said conductive member is formed of mainly W.

22. A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said capacitor dielectric film is deposited at a film deposition temperature of not greater than 500 degrees Celsius.

23. A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said capacitor dielectric film is deposited at a film deposition temperature of not greater than 475 degrees Celsius.

24. A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said capacitor dielectric film is formed by depositing a PZT film by a chemical vapor deposition process at a substrate temperature of not greater than 430 degrees Celsius.

25. A process for fabricating a semiconductor memory, claimed in Claim 15, wherein said capacitor dielectric film is formed by a sputtering or a solgel method.

26. A semiconductor memory including a capacitor formed on a semiconductor substrate and including a dielectric film formed between a first electrode and a second electrode opposing each other, a barrier layer being formed in contact with a surface of said first electrode opposite to said dielectric film, wherein said barrier layer has at least three layers, which include a first metal film, a metal nitride film and a second metal film.